# CMOS-compatible fabrication of bi-stable thin-film silicon membranes for quasi-perpetual piezoelectric energy harvester

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## ABSTRACT

In this paper we present the CMOS-compatible fabrication of the bi-stable silicon membrane that can be used for Energy Harvesting in micro-generator converting atmospheric pressure/temperature variations. Technological realization is industrially compatible to benefit from massive production and enable monolithic integration. The processing uses Silicon-On-Insulator technological platform and uses sequence of different layer depositions, both dielectric and metal, accompanied with wet and dry etching techniques. As a result a 1µm-thick various sized membranes are released. While the membrane is under-etched the internal residual stress in top silicon is released resulting in upward or downward membranes bending. Post-fabrication curvature of the membranes opens a possibility for sufficient bi-stable flexions that will be beneficial for energy production using piezoelectric materials. Atmospheric temperature/pressure variations are transformed to bi-stable membrane movements owing to liquid-to-vapour transitions of compound that fills the chamber below the membrane. This operational mode allows for harvesting energy from omnipresent daily changes of air temperature and pressure.

**Keywords:** Internet of Things, energy harvesting, piezoelectricity, temperature tides, quasi-perpetual energy harvesting, self-supplying, zero-power electronics

## 1. INTRODUCTION

Urged by worldwide increasing demand for energy[1], constrained by the growing amount of used battery waste[2] and challenged by unprecedented Internet of Things (***IoT***) markets growth[3], all industrially compatible solutions offering renewable energy play a strategic role. Energy Harvesting (***EH***)[4] converts waste or natural energy to produce electricity allowing to overcome aforementioned challenges and offering energy autonomy to ***IoT*** nodes and to the entire electronics. Decades of Moore's law[5]-driven development in the semiconductor industry flooded the market with smaller, cheaper, better-performing and less energy consuming devices opening new age of zero-power electronics[6]. Modern transistor requires a few atto-Joules (atto=$10^{-18}$J) of energy per switching[7] which is not zero but close enough to reach self-supply and battery-free operation. Moreover, regarding size, quantity and portability, moder electronics calls more than ever before for maintenance-free and environmentally-friendly supply techniques that can offer "*Drop it and forget it*" operation[8]. However, conventional *EH* techniques share same drawbacks: (***i***) intermitted energy production depending on source energy availability; (***ii***) performance dependence on input energy-to-harvester contact quality.. Therefore, a huge relief would be ***EH*** from omnipresent energy sources. Example of such source are natural atmospheric pressure and temperature variations (Fig. 1).

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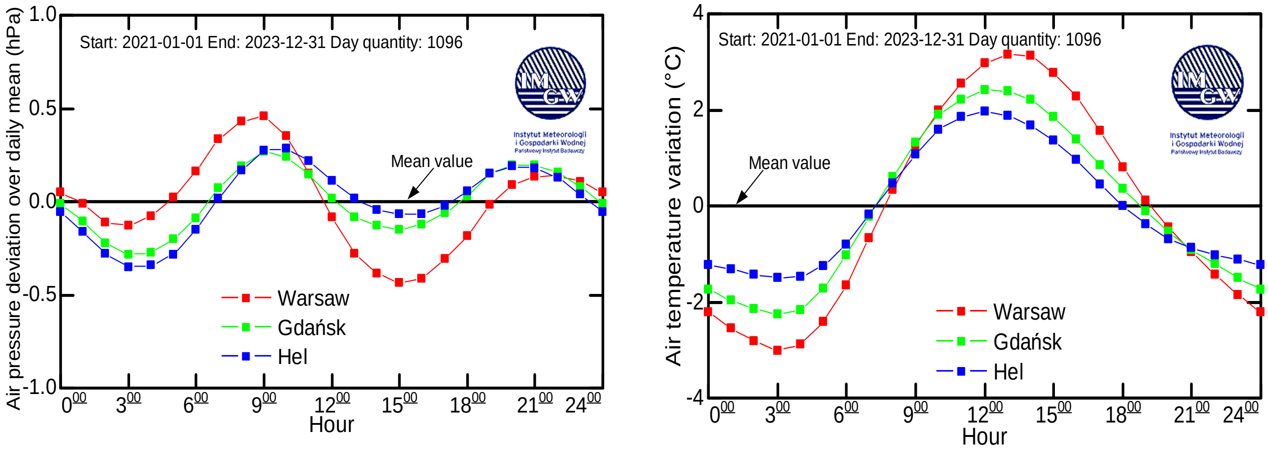



Figure 1. Atmospheric pressure and air temperature changes over day („*tides”*) for 3 cities in Poland [*Institute of Meteorology and Water Management – Polish Research Institute*].

Our innovative ***EH*** concept benefits from such omnipresent natural atmospheric/temperature variations to produce electricity – the SFINKS generator [9]. The idea uses temperature-induced vapour pressure dependance of a working fluid filling the chamber below the membrane leading to pressure changes under the bi-stable membrane resulting in abrupt flexions (see Fig. 2). Movements of the membrane are converted to electricity in piezoelectric material that is covering the membrane. Statistically, there are at least two flexions per day, constituting very attractive always- and everywhere delivering ***EH***.

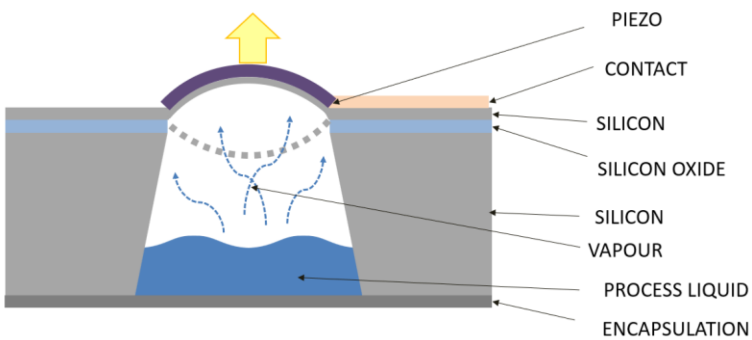



Figure 2. SFINKS harvester cross-sectional view.

Working fluid that can be used in this *EH* technique has to exhibit strong dependance of vapour-pressure against temperature. Fig. 3 compares vapour pressure of a different liquids and gases over temperature. Compound that fits this application the best is chloroethane - a liquid with low boiling point at 286K (12,3˚C) and high vapour pressure of 135kPa (at 20˚C) [10,11].

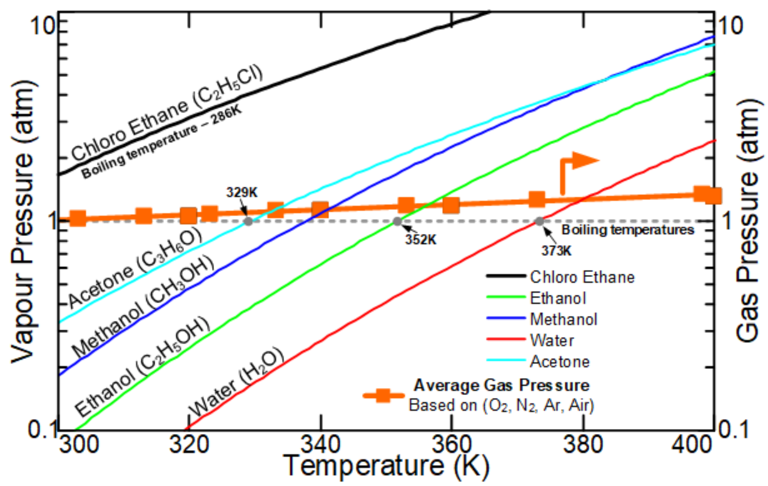


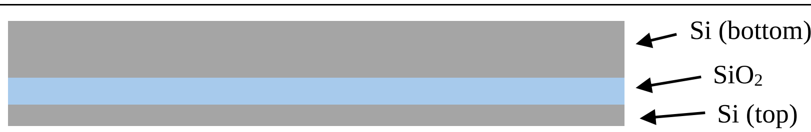
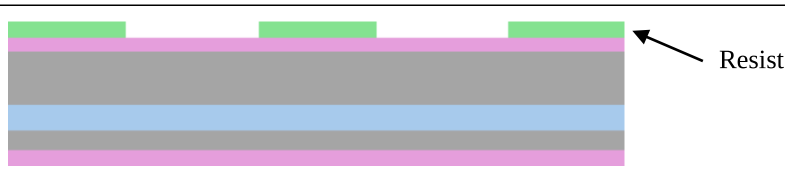

Figure 3. Dependance of vapour pressure versus temperature for different liquids and gasses[11].

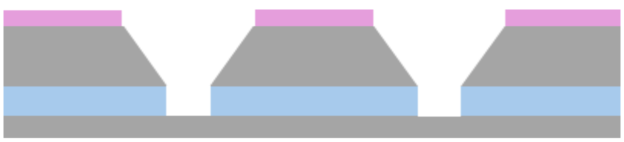
The opportunity offered by above-described physics and operation mode is to fabricate SFINKS engines on industrial scale. ***CMOS***-compatible fabrication can simultaneously produce big number of such generators and enable monolithic integration.

## 2. METHODS

Fabrication of the μ-membranes is performed using CMOS-compatible processes using 4" Silicon-On-Insulator (***SOI***) substrate. It has 1μm thick top Si layer, 1μm thick $SiO_2$ layer and Si hander with crystallographic orientation <100>. Both top and bottom sides of the wafer are polished.
Most of processing is done from the bottom side of the wafer therefore the orientation is swapped at the beginning.
The full process flow is presented in the Table 1.

Table 1. Process flow for manufacturing Si membranes.

| | | |
|---|---|---|
| a |  | 4in SOI wafer cleaning |
| b |  | $Si_xN_y$ deposition |
| c |  | Photolithography |

| | | |
|---|---|---|
| d |  | ICP etching |
| e |  | Resist removal (ICP) |
| f |  | KOH etching |
| g |  | SiN removal in ICP |
| h |  | Vapour HF etching |

Process starts with the SOI cleaning using Piranha solution, (3:1 96%$H_2SO_4$ with 30%$H_2O_2$) followed by native oxide removal in buffered oxide etchant solution (Tab. 1a).. Afterwards, a 120nm-thick low-stress silicon nitride ($Si_xN_y$) is deposited using Low Pressure Chemical Vapour Deposition (***LPCVD***) (Tab. 1b). $Si_xN_y$ layer will used as a protective layer in the during the processing. Subsequently, a photolithography is performed on the wafer's back-side (Tab. 1c) followed by Inductively Coupled Plasma (***ICP***) etching in $CHF_3$-$O_2$ atmosphere to selectively remove $Si_xN_y$ and expose the Si-handler (Tab. 1d). Remaining photoresist is stripped using $O_2$-based ***ICP*** etching (Tab. 1e). Next, the Si-hander is etched in 40% KOH solution at 80˚C (Tab. 1f). Such process is depending on ***Si*** crystalline orientation, highly Si/$SiO_2$ selective, and therefore naturally stops when reaching $SiO_2$ layer. Shape of the chamber is determined by the substrate crystalline orientation and in this case the etching results in trapezoid cavities with 54.74˚ (Fig. 4)[12,13].

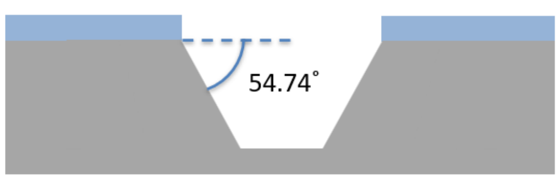



Figure 4. Si anisotropic etching in KOH.

Afterwards, the remaining top-side $Si_xN_y$ is removed in the ***ICP*** with the same process as before (Tab. 1 g). Finally, $SiO_2$ remaining below the top Si etched using ***HF*** vapours (Tab. 1h), and the membrane is totally released.

As the result of the performed processing steps a full matrix of membranes were achieved (Fig. 5)

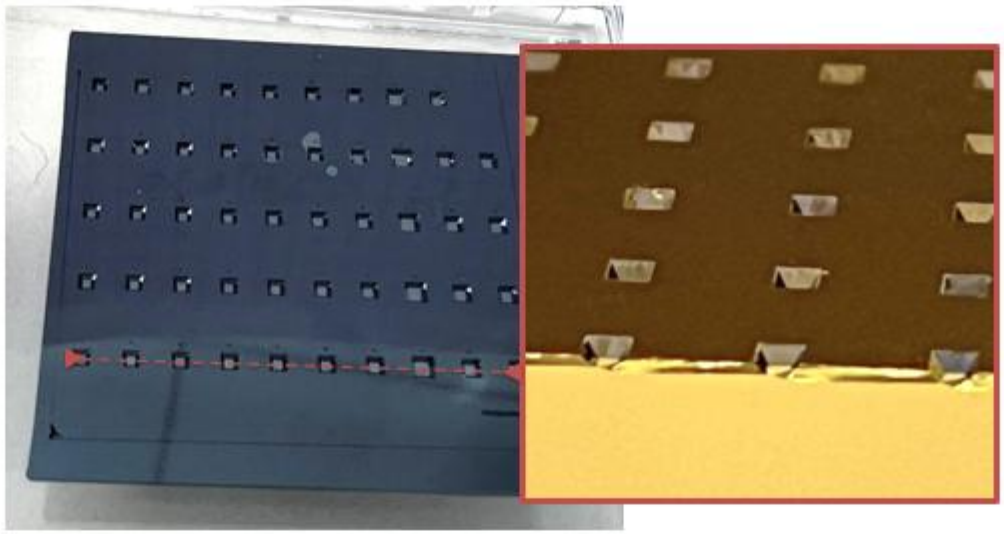


Figure 5. Fabricated chambers with released membranes.

## 3. RESULTS

We have developed processing of various-sized ***Si*** membranes. Proposed process flow is stable, repeatable and industrially compatible. Optical profilometer inspection (Rtec UP-3000, WLI) revealed that membranes are symmetrical along X-Y axis (Fig. 6). Due to the internal stress relaxation within the top silicon, the released membranes are naturally bend upwards or downwards.

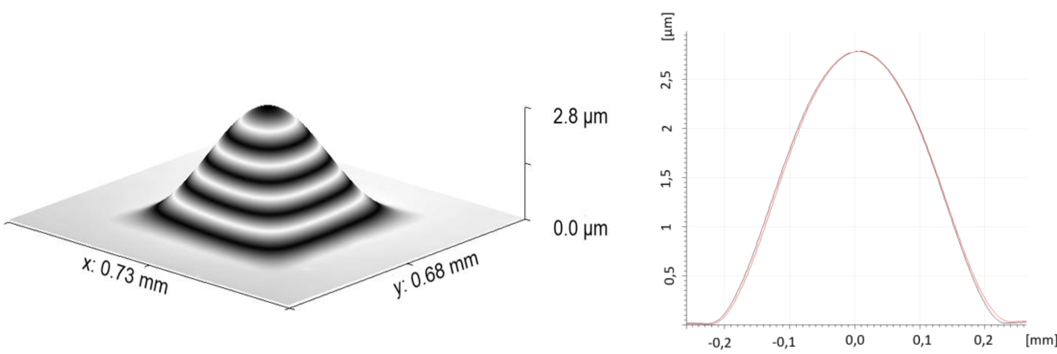



Figure 6. 3D map and X-Y profile of the fabricated membranes.

Variation of membrane's lateral dimensions allows for tuning the chamber volume, enabling tuning of the membrane flipping at given pressure/temperature.

## 4. SUMMARY

We report the development of ***CMOS***-compatible thin-film ***Si*** membrane release process. Reaching up to 100% yield confirms suitability for mass-scale production. Membranes are elastic and can withstand multiple flections. By attaching piezoelectric to the membrane and filling the cavity with the working fluid (*i.e. chloroethane*) a SFINKS generator is created. Such device can take advantage of the naturally occurring temperature/pressure fluctuations to generate electrical energy constituting ubiquitous powering for various electronic devices.

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